Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (cancelled)

2. (previously presented) An output buffer, comprising:

a first circuit coupled between a first power line and a pad; and

a second circuit coupled between a second power line and the pad, the second circuit comprising:

a resistor constructed by a well region of a second conductivity type disposed on a substrate of a first conductivity type, the resistor comprising a first end and a second end, the first end being a doped region of the second conductivity type at least partially overlapping the well region and coupled to the pad;

a first doped region of the first conductivity type disposed within the well region;

a capacitor coupled between the pad and the first doped region; and

an electrostatic discharge protection component, coupled between the second end and the second power line.

3-4. (cancelled)

5-7. (withdrawn)

8-10. (cancelled)

11-12. (withdrawn)

13. (cancelled)

14. (cancelled)

15-30. (withdrawn)

31. (cancelled)

32-33. (withdrawn)

34. (previously presented) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first doped region and the second doped region being spaced apart enabling a channel region formed in between;

a well region of the second conductivity type, formed in the substrate; and

a fourth doped region and a fifth doped region of the second conductivity type formed in the well region, the fourth doped region coupled to the first node; and

a third doped region of the first conductivity type disposed within the well region, wherein the third doped region is electrically floated and is spaced apart from the fourth doped region, the first node is electrically coupled to the first doped region through the fourth doped region, the well region, and the fifth doped region, and the second node is

electrically coupled to the second doped region.

35-37. (cancelled)

38. (previously presented) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first and second doped regions being spaced apart enabling a channel formed in between;

a resistor constructed by a well region of a second conductivity type being disposed on the substrate, the resistor comprising a fourth doped region and a fifth doped region of the second conductivity type; the fourth doped region coupled to the first node; and

a third doped region of the first conductivity type disposed within the well region, wherein the third doped region is coupled to the first node through a capacitor; the third doped region is spaced apart from the fourth doped region; the first node is electrically coupled to the first doped region through the fourth doped region, the well region, and the fifth doped region; and the second node is electrically coupled to the second doped region.

39-42. (cancelled)

43. (previously presented) The electrostatic discharge protection circuit of claim 34, wherein the third doped region is electrically floating between the fourth doped region and the

fifth doped region.

44. (previously presented) The electrostatic discharge protection circuit of claim 34, wherein the third doped region is spaced apart from the fifth doped region.

45. (previously presented) The electrostatic discharge protection circuit of claim 34, wherein the fifth doped region is at least partially overlapping with the well region.

46. (previously presented) The electrostatic discharge protection circuit of claim 38, wherein the third doped region is disposed between the fourth doped region and the fifth doped region.

47. (previously presented) The electrostatic discharge protection circuit of claim 38, wherein the third doped region is spaced apart from the fifth doped region.

48-60. (cancelled)

61. (previously presented) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first doped region and the second doped region being spaced apart enabling a channel region formed in between;

a well region of the second conductivity type formed in the substrate;

a third doped region of the second conductivity type formed in the well region and coupled to the first node; and

a fourth doped region of the first conductivity type disposed within the well region, wherein the fourth doped region is electrically floated and is spaced apart from the third doped region, the first node is electrically coupled to the first doped region through the third doped region and well region; and, the second node is electrically coupled to the second doped region.

62. (previously presented) The electrostatic discharge protection circuit of claim 61, further comprising a fifth doped region of the second conductivity type disposed in the well region, wherein the fourth doped region is electrically floating between the third doped region and the fifth doped region.

63. (previously presented) The electrostatic discharge protection circuit of claim 62, wherein the fourth doped region is spaced apart from the fifth doped region.

64. previously presented) The electrostatic discharge protection circuit of claim 62, wherein the fifth doped region is at least partially overlapping with the well region.

65. (previously presented) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductivity type;

a first doped region and a second doped region of a second conductivity type formed in the substrate, the first and second doped regions being spaced apart enabling a channel formed in

between;

a well region of the second conductivity type formed in the substrate; and

a third doped region of the second conductivity type disposed in the well region and coupled to the first node;

a fourth doped region of the first conductivity type disposed within the well region, wherein the fourth doped region is coupled to the first node through a capacitor; wherein

the fourth doped region is spaced apart from the third doped region; the first node is electrically coupled to the first doped region through the third doped region and the well region; and the second node is electrically coupled to the second doped region.

66. (previously presented) The electrostatic discharge protection circuit of claim 65, further comprising a fifth doped region of the second conductivity type disposed in the well region, and coupled to the second doped region.

67. (previously presented) The electrostatic discharge protection circuit of claim 65, wherein the fourth doped region is disposed between the third doped region and the fifth doped region.

68. (previously presented) The electrostatic discharge protection circuit of claim 65, wherein the fourth doped region is spaced apart from the fifth doped region.

69-74. (cancelled)